ITI LIMITED
Palakkad Plant, Kanjikode West
PALAKKAD – 678 623
KERALA –INDIA

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Ref: PN490I008 Date : 13.10.2020

Dear Sir,

Sub: Request for Quote – Electronic Components

ITI Limited, Palakkad Plant requires 5Types Electronic Components for our AMC department . The Details of items are as follows.

Sl. No	Item Code	Description	H S N	Qty
1	501R000603	SMD 0603 RES 1R00 1% 100PPM 50V 0.1W	85.42.31.00	5000 Nos.
2	50331R0603	SMD 0603 RES 331R 1% 100PPM 50V 0.1W	85.42.31.00	5000 Nos.
3	50LM5026MTX	LM5026 ACTIVE CLAMPCURRENT MODE PWM CONTROLLER 16 PIN TSSOP PACKAGE	85.42.31.00	250 Nos.
4	50MMBT3904LT1	MMBT3904LT1 SOT-23 PLASTIC ENCAPSULATED TRANSISTORS	85.42.31.00	500 Nos.
5	50SI7898DP	SI 7898 DP N-CHANNEL 150V (D-S) MOSFET Power PAK SO-8 SINGLE	85.42.31.00	500 Nos.

Please submit your most competitive Offer for the above items showing the Item Code, Description, Date Code , Make, Part No, MOQ/MPQ etc in the following address in a sealed envelope to reach us on or before the due date on 21.10.2020 at 5.00 pm. E-mail quotes are also acceptable.

THE DEPUTY GENERAL MANAGER (MM)
ITI Ltd., Kanjikode West. P. O
Palakkad- 678 623,Tel: 0491 2566511.
The mail ID for general correspondence/queries / clarifications : pur3_pkd@itiltd.co.in

GENERAL TERMS & CONDITIONS

1. Terms of price : At our Stores
2. Due date : 21.10.2020 at 05.00 pm.
3. Tender opening date : 22.10.2020 at 02.30 pm.
4. Validity of the quote : 120 days.
5. Packing : Standard packing
7. Payment : 100 % within 90 days from date of delivery and Acceptance
8. Delivery : Immediate

PLEASE INDICATE THE RFQ REFERENCE ,PN490I008 and DUE DATE i.e., 21-10-2020 – On top of the envelope of your quotation. *Quote should be in INR*. Please acknowledge the receipt of this enquiry by return mail. The interested bidders can participate in the tender opening.

Kindly attach copy of relevant documents if your firm is registered with MSME and NSIC for the availing the benefits extended to the MSEs.

Thanking You
Yours faithfully

13.10.2020
C.USHA
Dy. Gen. Manager (MM)

SPEC: SL. NO. 3

TEXAS INSTRUMENTS

LM5026

SNVS363E – AUGUST 2005 – REVISED NOVEMBER 2015

LM5026 Active Clamp Current Mode PWM Controller

1 Features

- Current-Mode Control
- Internal 100-V Start-Up Bias Regulator
- 3-A Compound Main Gate Driver
- High Bandwidth Optocoupler Interface
- Programmable Line Undervoltage Lockout (UVLO) With Adjustable Hysteresis
- Versatile Dual Mode Overcurrent Protection With Hiccup Delay Timer
- Programmable Overlap or Deadtime between the Main and Active Clamp Outputs
- Programmable Maximum Duty Cycle Clamp
- Programmable Soft-Start
- Leading Edge Blanking
- Resistor Programmed 1-MHz Capable Oscillator
- Oscillator Sync I/O Capability
- Precision 5-V Reference

2 Applications

- Server Power Supplies
- 48-V Telecom Power Supplies
- High Efficiency DC–DC Power Supplies

3 Description

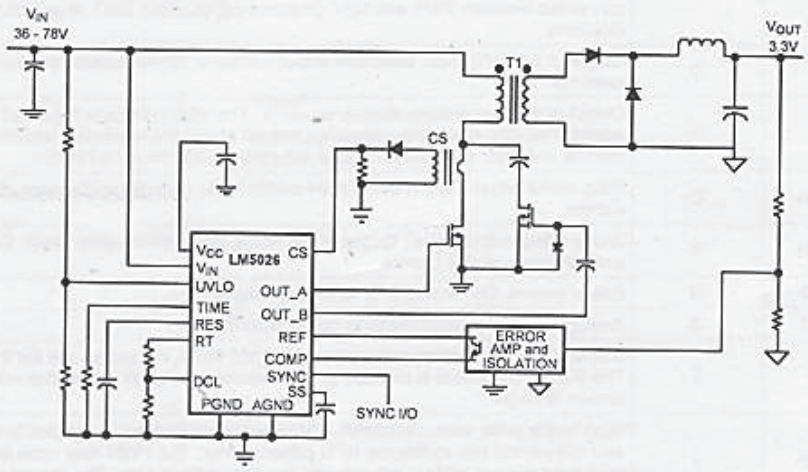
The LM5026 PWM controller contains all of the features necessary to implement power converters utilizing the active clamp and reset technique with current-mode control. With the active clamp technique, higher efficiencies and greater power densities can be realized compared to conventional catch winding or RDC clamp and reset techniques. Two control outputs are provided, the main power switch control (OUT_A) and the active clamp switch control (OUT_B). The device can be configured to control either a P-Channel or N-Channel clamp switch. The main gate driver features a compound configuration, consisting of both MOS and Bipolar devices, providing superior gate drive characteristics. The LM5026 can be configured to operate with bias voltages over a wide input range of 8 V to 100 V. Additional features include programmable maximum duty cycle, line undervoltage lockout, cycle-by-cycle current limit, hiccup mode fault operation with adjustable timeout delay, PWM slope compensation, soft-start, 1-MHz capable oscillator with synchronization input and output capability, precision reference, and thermal shutdown.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM5026	WSON (16)	5.00 mm × 5.00 mm
	TSSOP (16)	4.40 mm × 5.00 mm

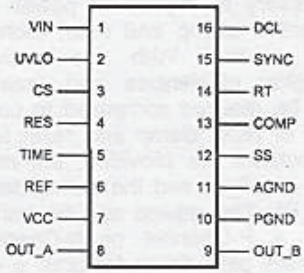
(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



5 Pin Configuration and Functions

PW Package
16-Pin TSSOP
Top View



NHQ Package
16-Pin WSON
Top View

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	VIN	I	Input voltage source. Input to the start-up regulator. Operating input range is 13 V to 100 V with transient capability to 105 V. For power sources outside of this range, the LM5026 can be biased directly at VCC by an external regulator.
2	UVLO	I	Line undervoltage lockout. An external voltage divider from the power source sets the shutdown and standby comparator levels. When UVLO reaches the 0.4-V threshold the VCC and REF regulators are enabled. At the 1.25-V threshold the SS pin is released and the device enters the active mode.
3	CS	I	Current Sense input for current mode control and current limit. If CS exceeds 0.5 V, the output pulse will be terminated, entering cycle-by-cycle current limit. An internal switch holds CS low for 100 nS after OUT_A switches high to blank leading edge transients.
4	RES	I	Restart Timer. If cycle-by-cycle current limit is reached during any cycle, a 10-µA current is sourced to the RES pin capacitor. If the RES capacitor voltage reaches 2.5 V, the soft-start capacitor will be fully discharged and then released with a pullup current of 1 µA. After the first output pulse at OUT_A (when SS = 1.4 V), the SS pin charging current will revert back to 50 µA.
5	TIME	I	Gate drive overlap or deadtime control. An external resistor (RSET) sets either the overlap time or deadtime for the active clamp output. An RSET resistor connected between TIME and AGND produces in-phase OUT_A and OUT_B pulses with overlap. An RSET resistor connected between TIME and REF produces out-of-phase OUT_A and OUT_B pulses with deadtime.
6	REF	O	Output of 5-V reference. Maximum output current is 10 mA. Locally decouple with a 0.1-µF capacitor.
7	VCC	P	Output of the high voltage start-up regulator. The VCC voltage is regulated to 7.6 V. If an auxiliary winding raises the voltage on this pin above the regulation setpoint, the internal start-up regulator will shutdown, thus reducing the IC power dissipation.
8	OUT_A	O	Main output driver. Output of the main switch PWM gate driver. Capable of 3-A peak sink current.
9	OUT_B	O	Active clamp output driver. Output of the active clamp switch gate driver. Capable of 0.5-A peak source and sink current.
10	PGND	G	Power ground. Connect directly to analog cround.
11	AGND	G	Analog return. Connect directly to power cround.
12	SS	I	Soft-start. An external capacitor and an internal 50-µA current source set the soft-start ramp. The SS current source is reduced to 1 µA following a restart event. The soft-stop discharge current is 50 µA.
13	COMP	I	Input to the pulse width modulator. The external optocoupler connected to the COMP pin sources current into an internal NPN current mirror. The PWM duty cycle is maximum with zero input current, while 1 mA reduces the duty cycle to zero. The current mirror improves the frequency response by reducing the ac voltage across the optocoupler detector.

(1) P = Power, G = Ground, I = Input, O = Output, I/O = Input/Output

Spec: SL-NO. 4

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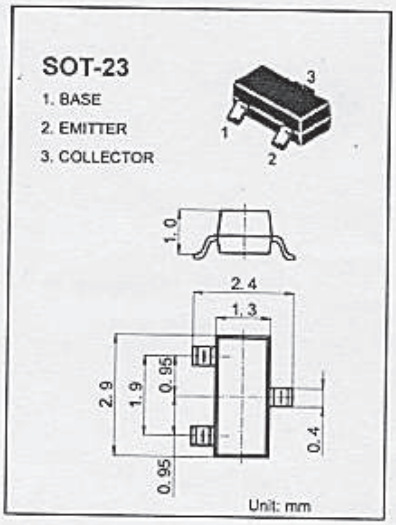
MMBT3904LT1

SOT-23 Plastic-Encapsulate Transistors

MMBT3904LT1 TRANSISTOR (NPN)



FEATURES

Power dissipation

P_{CM}: 0.2 W (Tamb=25℃)

Collector current

I_{CM}: 0.2 A

Collector-base voltage

$V_{(BR)CBO}$: 60 V

Operating and storage junction temperature range

T_J, T_{stg}: -55℃ to +150℃

ELECTRICAL CHARACTERISTICS (Tamb=25℃ unless otherwise specified)

Parameter	Symbol	Test conditions	MIN	MAX	UNIT
Collector-base breakdown voltage	$V_{(BR)CBO}$	I_C= 100 μA, I_E=0	60		V
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	I_C= 1 mA, I_B=0	40		V
Emitter-base breakdown voltage	$V_{(BR)EBO}$	I_E= 100μA, I_C=0	6		V
Collector cut-off current	I_{CBO}	V_{CB}= 60V, I_E=0		0.1	μA
Collector cut-off current	I_{CEO}	V_{CE}= 40V, I_B=0		0.1	μA
Emitter cut-off current	I_{EBO}	V_{EB}= 5V, I_C=0		0.1	μA
DC current gain	$H_{FE(1)}$	V_{CE}=10V, I_C= 1mA	100	300	
	$H_{FE(2)}$	V_{CE}= 1V, I_C= 50mA	60		
Collector-emitter saturation voltage	V_{CE}(sat)	I_C=50mA, I_B= 5mA		0.3	V
Base-emitter saturation voltage	V_{BE}(sat)	I_C= 50mA, I_B= 5mA		0.95	V
Transition frequency	f_T	V_{CE}= 20V, I_C= 10mA f=100MHz	250		MHz
Delay Time	td	V_{CC}=3.0Vdc, V_{BE}=-0.5Vdc I_C=10mAdc, I_{B1}=1.0mAdc		35	nS
Rise Time	tr			35	nS
Storage Time	ts	V_{CC}=3.0Vdc, I_C=10mAdc I_{B1}=I_{B2}=1.0mAdc		200	nS
Fall Time	tf			50	nS

DEVICE MARKING

MMBT3904LT1=1AM

Website http://www.avictek.com

Spec: SL. NO. 5
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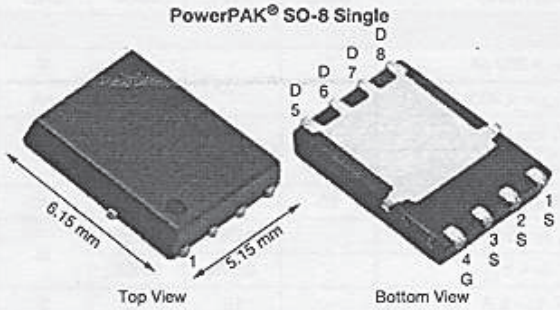
VISHAY.
www.vishay.com

Si7898DP
Vishay Siliconix

N-Channel 150 V (D-S) MOSFET

PowerPAK® SO-8 Single



Top View | Bottom View

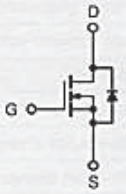
FEATURES

- TrenchFET® power MOSFETs for fast switching
- New low thermal resistance PowerPAK® package with low 1.07 mm profile
- PWM optimized
- 100 % R_g tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE Available

APPLICATIONS

- DC/DC power supply primary side switch
- Industrial motor drives



N-Channel MOSFET

PRODUCT SUMMARY	
V_{DS} (V)	150
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.085
$R_{DS(on)}$ max. (Ω) at V_{GS} = 6 V	0.095
Q_g typ. (nC)	17
I_D (A)	4.8
Configuration	Single

ORDERING INFORMATION	
Package	PowerPAK SO-8
Lead (Pb)-free	Si7898DP-T1-E3
Lead (Pb)-free and halogen-free	Si7898DP-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	10 s	STEADY STATE	UNIT
Drain-source voltage		V_{DS}	150	150	V
Gate-source voltage		V_{GS}	± 20	± 20	
Continuous drain current (T_J = 150 °C) [a]	T_A = 25 °C	I_D	4.8	3	A
	T_A = 70 °C		3.8	2.4	
Pulsed drain current		I_{DM}	25	25	
Avalanche current	L = 0.1 mH	I_{AS}	10	10	
Continuous source current (diode conduction) [a]		I_S	4.1	1.6	
Maximum power dissipation [a]	T_A = 25 °C	P_D	5	1.9	W
	T_A = 70 °C		3.2	1.2	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150		°C
Soldering recommendations (peak temperature) [b, c]			260		

THERMAL RESISTANCE RATINGS

PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient [a]	t ≤ 10 s	R_{thJA}	20	25	°C/W
	Steady state		52	65	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	2.1	2.6	

Notes

a. Surface mounted on 1" x 1" FR4 board
b. See solder profile (www.vishay.com/doc?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
c. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components

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Spec: SL.No.5

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Gate threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	2	-	4	V
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	± 100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 150 V, V_{GS} = 0 V	-	-	1	µA
		V_{DS} = 150 V, V_{GS} = 0 V, T_J = 55 °C			5	
On-state drain current [a]	$I_{D(on)}$	V_{DS} ≥ 5 V, V_{GS} = 10 V	25	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 3.5 A	-	0.068	0.085	Ω
		V_{GS} = 6 V, I_D = 3 A	-	0.076	0.095	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 5 A	-	15	-	S
Diode forward voltage [a]	V_{SD}	I_S = 2.5 A, V_{GS} = 0 V	-	0.75	1.2	V
Dynamic [b]						
Total gate charge	Q_g	V_{DS} = 75 V, V_{GS} = 10 V, I_D = 3.5 A	-	17	21	nC
Gate-source charge	Q_{gs}		-	3.2	-	
Gate-drain charge	Q_{gd}		-	6	-	
Gate resistance	R_g		0.5	0.85	2.5	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 75 V, R_L = 21 Ω I_D ≡ 3.5 A, V_{GEN} = 10 V, R_g = 6 Ω	-	9	14	ns
Rise time	t_r		-	10	15	
Turn-off delay time	$t_{d(off)}$		-	24	35	
Fall time	t_f		-	17	25	
Source-drain reverse recovery time	t_{rr}	I_F = 2.5 A, di/dt = 100 A/µs	-	45	70	

Notes

a. Pulse test: pulse width ≤ 300 µs, duty cycle ≤ 2 %

b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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